MEMS Fabrication of Silicon Ion Trap Arrays*

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Achieving practical quantum information processing with trapped ions requires large scale ion trap arrays. The scalable fabrication of ion trap arrays involves advanced nanofabrication techniques including photolithography. In the recently operated multi-layer gallium-arsenide integrated ion chip of Ref [1], voltages applied to the trap electrodes are limited by the type and thickness of the insulator material, resulting in a relatively shallow trapping potential (0.08eV). While the Ga-As system is suitable for ion trap scaling, the use of other materials[2] commonly used in micro-and nano-fabrication may be more advantageous, in particular the use of MEMS (micro-electromechanical system) silicon structures. Free standing structures, that are a typical feature of MEMS devices, appear particularly attractive as they permit larger voltages to be applied.

We report on the progress of the fabrication and design of fully integrated and monolithic MEMS silicon ion trap arrays. Electrodes are grown on a silicon chip, with thin insulating Si_3N_4 and SiO_2 layers isolating the electrodes while providing mechanical strength. The electrodes are fabricated by growing p-doped polysilicon and SiO_2 and removing the oxide layer between electrodes. The characteristic size of the proposed structure is in the 10-100 μm range. The dielectric and mechanical characteristics of SiO_2 and Si_3N_4 are expected to support high electrical potentials and low rf loss, with expected breakdown voltages exceeding 100V across a 0.5 μm gap and minimal heat dissipation. Pristine silicon and polysilicon structures may exhibit minimal surface irregularities, which may temper electrical noise that can adversely affect the trapped ion qubits[3,4]. The design also incorporates the possibility of on-board integrated capacitors and resistors, minimizing the amount of manual connections that need to be made to the chip.

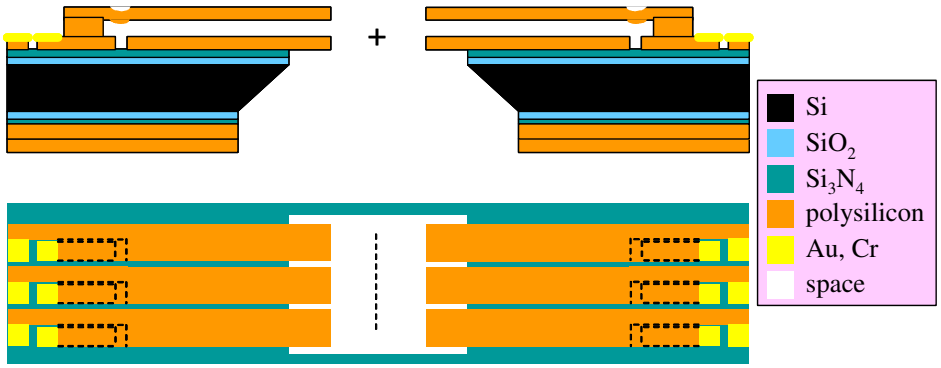

Fig. 1: Schematic of the silicon ion trap (not to scale). TOP: Cross section of back-etched silicon substrate and free-standing cantilevered polysilicon electrodes, spaced by insulating SiO_2 layer and Si_3N_4. Gold electrode bond pads allow the application of appropriate rf and static potentials. Electrode and insulating layers of order 1 μm thick. BOTTOM: Top view of trap structure, showing three axial sections (12 electrodes, 1 zone).

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