

A universal vacuum system for chip ion traps

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We have developed a modular vacuum system that can accommodate up to 48 DC control electrodes, allows for large beam access, and is capable of supporting both micro-fabricated symmetric linear quadrupole traps [1] as well as surface-electrode ion traps [2, 3]. Our system uses a custom socket for receiving a ceramic pin grid array chip carrier upon which we mount the ion trap. The socket consists of two UHV-compatible DuPont Vespel plates sandwiching 48 receptacles for the chip carrier. We mount the socket on a plate that supports radiofrequency (RF) filters on the back. By using this socket, the vacuum system has a low turn-around time, because the traps are “swappable.” When exchanging ion traps, we remove the chip carrier containing the old trap and plug in the new ion trap.

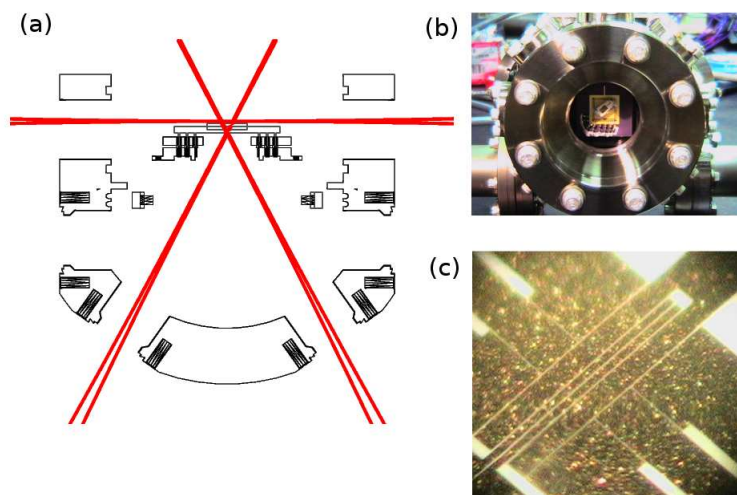


FIGURE 1:

(a) Schematic indicating the beam access for both the symmetric linear quadrupole traps and the asymmetric surface-electrode traps. (b) A photograph of a surface trap on a chip carrier, mounted in the vacuum chamber. (c) Close-up view of the surface trap. The outer electrodes are segmented, allowing for axial confinement; the middle electrodes rotate the principle axes of the trap via differential static biasing [4].

This vacuum system is not limited to ion traps that employ a through hole for laser access. Asymmetric surface-electrode ion traps, where the electrodes are located asymmetrically about the ion, such as proposed in [2] and recently demonstrated in [3] require laser beams to run parallel and close to the trap surface. We house the socket and ion trap inside a combination of a hemisphere and an octagon, providing ample beam access for both symmetric through traps as well as the asymmetric surface traps. In order to explore asymmetric ion trap geometries, we have installed a surface-electrode ion trap, mounted on a chip carrier (Figure 1b). Using photolithographic techniques, we deposited six gold electrode rails on an alumina substrate. The outer segmented electrodes provide axial confinement, and differential static biasing of the middle electrodes allow appropriate rotation of the principle axes (Figure 1c) [4]. An applied RF voltage of 250V will result in a trap depth of $0.25eV$. We report progress in trying to load ions into the trap.

Future studies will incorporate the implementation of multiple zones and junctions on chip traps for both geometries — symmetric through traps as well as asymmetric surface-electrode traps. Additionally we will investigate novel junctions that may suppress or eliminate RF humps.

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[1] D. Stick, et. al., *Nature Physics* **2** 36 (2006)

[2] J. Chiaverini, et. al. *Quantum Inf. Comput.* **5**, 419 (2005)

[3] S. Seidelin, et. al. *e-print* quant-ph/0601173

[4] From discussions with M. Madsen