Semiconductor Fabrication of Ion Traps

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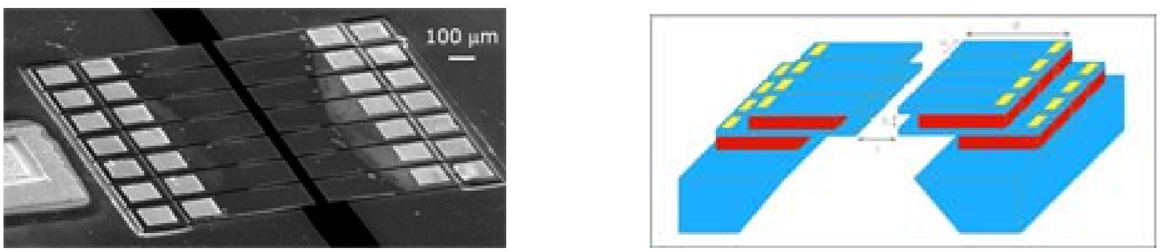
Semiconductor processing techniques, particularly photolithography on integrated structures, allows for the fabrication of ion traps which can in principle host large numbers of qubits and shuttle ions between many separated trapping zones. Here we discuss the trapping of a single ion in an rf linear Paul trap, fabricated on a monolithic gallium arsenide (GaAs) heterostructure. The trap consists of four alternating layers of AlGaAs and doped GaAs on a GaAs substrate, where the doped GaAs forms the cantilevers to which rf and dc voltages are applied, and the AlGaAs serves to insulate and isolate the GaAs cantilevers. The first step in the process uses a wet etch to remove material from the backside of the substrate for optical access. Next cantilevers are patterned photolithographically on the top side and etched with a dry etch, and bond pads are laid down to make electrical connections to the cantilevers. Finally, an HF etch removes insulating material from between the cantilevers. In addition to the processing steps, we discuss the technical difficulties arising from the restrictive electrical characteristics of the trap, primarily voltage breakdown. We also present the heating measurement for a single ion in the trap, which is calculated by measuring the suppression of the Raman carrier transition rate, and speculate on possible sources of the anomalously high heating rate.



(a) (b)

Fig. 1: (a). SEM image of a GaAs trap (b). Rendition of the structure with disproportionate dimensions in order to show layer structure. The blue parts are GaAs, the red parts are AlGaAs, and the gold parts are Ni/Ge/Au bondpads.

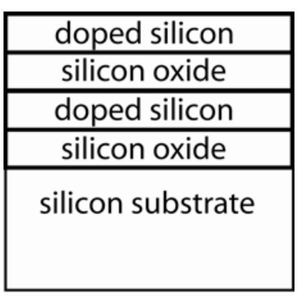


Fig. 2: Using recently developed techniques, a Si/SiO_2 substrate can be constructed with a similar layer structure as the MBE grown GaAs/AlGaAs trap. The advantage of Si/SiO_2 is that larger voltages can potentially be applied, given the superior insulating properties of SiO_2.

Given the limitations which material properties place on the operation of semiconductor ion traps, we discuss another possible fabrication technique for constructing symmetric ion traps. This avenue uses a Si/SiO_2 heterostructure which closely resembles the GaAs/AlGaAs heterostructure above. The superior insulating properties of SiO_2 would allow for larger voltages and therefore higher trap depths.

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